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EXAMINER

HOLLINGTON, JERMELE M

ART UNIT	PAPER NUMBER
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2829

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/529,340	Applicant(s) FISCHER ET AL.	
	Examiner Jermele M. Hollington	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 December 2006.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-9,11-14 and 17-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-7,9,11-14 and 17-25 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, an integrated circuit substrate [claim 1] must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: there are no section heading in the disclosure such as TITLE OF THE INVENTION, BACKGROUND OF THE INVENTION, BRIEF SUMMARY OF THE INVENTION, BRIEF DESCRIPTION OF THE

SEVERAL VIEWS OF THE DRAWING(S), DETAILED DESCRIPTION OF THE
INVENTION, and CLAIM OR CLAIMS.

Appropriate correction is required.

Claim Objections

3. Claim 1 is objected to because of the following informalities: in line 2 of the amending claim 1, the limitation "a integrated circuit" should be change to --an integrated circuit--.

Furthermore, the disclosure does not show an integrated circuit substrate. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-4, 6-7, 9, 11-14, 17-18 and 20-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Jaimsomporn et al (6392432).

Regarding claims 1 and 13, Jaimsomporn et al disclose [see Fig. 3] an integrated test circuit arrangement (system 300) having integrated test structures (sockets 112, 114, 116) at least one integrated heating element (heating element 106), an integrated detection unit (signal measurement unit 302) which detects at least one physical property for each of the test structures (112, 114, 116), an integrated supply unit (power supply 132), which supplies each of the test

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structures (112, 114, 116) with a current or a voltage in switchable fashion independently of one another, and a control unit (processing unit 304) which is connected to outputs of the detection unit (302) on an input side and which controls the supply unit (132) dependent on the detection results.

Regarding claims 3 and 18, Jaimsomporn et al disclose wherein the test structures (112, 114, 116) of a first group have the same construction among one another (see Fig. 3).

Regarding claim 4, Jaimsomporn et al disclose wherein at least one of: the supply unit (132) contains at least one of: a multiplicity of integrated current sources and a multiplicity of integrated voltage sources, and the current sources contain a plurality of current mirrors which generate a multiple or a fraction of a reference current or a current having the magnitude of the reference current.

Regarding claim 6, Jaimsomporn et al disclose at least one reference structure (118), at least one of the construction and the dimensions of which differ from the construction and the dimensions of the test structures (112, 114 116).

Regarding claim 7, Jaimsomporn et al disclose wherein the detection unit (302) at least one of: is connected or can be connected to the test structures (112, 114, 116), and contains at least one counter, which is clocked in accordance with a predetermined clock.

Regarding claim 9, Jaimsomporn et al disclose the control unit (304) outputs at least one of: detection results, a datum for ascertaining the detection instant and which, datum for identifying the test structures (112, 114, 116).

Regarding claim 11, Jaimsomporn et al disclose electronic components (308 and 310) associated with a user circuit (304).

Regarding claim 12, Jaimsomporn et al disclose wherein the circuit arrangement (102) is encapsulated in a plastic housing or in a ceramic housing (housing 104).

Regarding claim 14, Jaimsomporn et al disclose comprising at least one of the following steps: integrating at least one heating element (106) into the integrated circuit arrangement (102), warming or heating the test structures (112, 114, 116) with the aid of the heating element (106), and connecting the supply unit (132) to the test structure (112, 114, 116) during warming or during heating.

Regarding claim 17, Jaimsomporn et al disclose further comprising the following steps: integrating at least one reference structure (118), at least one of the construction and the dimensions of which differ from the construction and the dimensions of the test structures (112, 114, 116), detecting one of the physical reference properties at the reference structure (118), comparing (via 302) the one of the physical properties with the reference property or comparing (via 302) a quantity generated from the one of the physical properties and a quantity generated from the reference property.

Regarding claim 20, Jaimsomporn et al disclose an output circuit (122) is integrated into the integrated circuit arrangement (102), the output circuit (122) outputs at least one set of detection data for the test structures (112, 114, 116).

Regarding claim 21, Jaimsomporn et al disclose at least one of: an integrated circuit arrangement (102) that is still arranged on a semiconductor wafer (102), the semiconductor wafer (102) carrying a multiplicity of other integrated circuit arrangements (118, 120, 122), and in that the method for the purpose of monitoring ongoing production.

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Regarding claim 22, Jaimsomporn et al disclose integrating at least a part of the supply unit (132) into the integrated circuit arrangement (102), said part containing at least one active component.

Regarding claim 23, Jaimsomporn et al disclose the test structures (112, 114 or 116) of a second group contain interconnects which at least one of: comprise a metal or are led into another metallization layer by means of a via, the test structures (112, 114 or 116) of a third group contain dielectrics, or the test structures (112, 114, or 116) of a fourth group contain active or passive electronic components.

Regarding claim 24, Jaimsomporn et al disclose the electronic components (308 and 310) comprise at least one of a memory unit (308) and a processor (shown not numbered).

Regarding claim 25, Jaimsomporn et al disclose registering an instant at which the comparison result changes.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

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the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaimsomporn et al (6392432) in view of Soh et al (6060895).

Regarding claim 5, Jaimsomporn et al disclose the heating element (106). However, they do not disclose the detail of the heating element as claimed. Soh et al disclose a heating element (heating element 11) comprises at least one of: contains a resistance heating element which comprises monocrystalline silicon or polycrystalline silicon (see col. 5, lines 64-66) or which comprises a metal (see col. 5, lines 64-66), and has a straight profile, a meandering profile, a triangular function profile or a rectangular function profile (see Fig. 1 or 5). Further, Soh et al teach that the addition of heating element made out of the materials above is advantageous because it provides localized heating of selected portions of the IC and to make the heating element an effective resistive heating element. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Jaimsomporn et al by adding monocrystalline silicon or polycrystalline silicon or a metal to the heating element as taught by Soh et al in order to localized heating of selected portions of the IC and to make the heating element an effective resistive heating element.

Regarding claim 19, Jaimsomporn et al disclose the heating element (106) is at least one of: fed with at least one of an AC current and a DC current. However, they do not disclose the heating element is heated to temperatures of greater than two hundred degrees Celsius. Soh et al disclose a heating element (heating element 11) that is heated to temperatures of greater than two

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hundred degrees Celsius [see col. 4 and col. 7, lines 49-55]. Further, Soh et al teach that the addition of heating element heated to over 200 degrees Celsius is advantageous because it provides the localized heat at the wafer level directly to the vicinity of the dielectric element to be tested and to be used to produce breakdown in 10 seconds or less. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Jaimsomporn et al by adding more than 200 degrees Celsius to the heating element as taught by Soh et al in order to provides the localized heat at the wafer level directly to the vicinity of the dielectric element to be tested.

Conclusion

Response to Arguments

9. Applicant's arguments filed December 26, 2006 have been fully considered but they are not persuasive.

A) The applicants' argue: "Jaimsomporn does not teach these elements as being part of an integrated circuit arrangement or on the same integrated circuit substrate."

In response to the above argument, the prior art shows in Fig. 3 that all of the elements are part of the system 300. Therefore, the examiner believes the prior art still read on the claimed invention.

B) The applicants' further argues: "Soh does not teach or suggest the elements noted above as missing from Jaimsomporn."

In response to the above argument, 1) Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably

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distinguishes them from the references. 2) Applicant's arguments do not comply with 37 CFR 1.111(c) because they do not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. 3) In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

10. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 8, the primary reason for the allowance of the claim is due the detection unit contains at least one multiplexer unit, the inputs of which are electrically connected to a respective test structure, and in that the an output of the multiplexer unit is connected to the first input of a comparison unit, the second input of which is electrically connected to a reference structure, the reference structure having at least one of a different construction and different dimensions than a-the test structures.

Base on the arguments above the following is being applied.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:00 EST) First Friday Off.

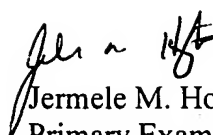
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Jermele M. Hollington
Primary Examiner
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JMH

March 15, 2007